Critical Evaluation of IGBT Performance in Zero Current Switching Environment

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Abstract - This paper reports the internal carrier dynamics of IGBT under Zero Current Switching conditions. ZCS performance of a punch-through IGBT is studied with the aid of extensive measurements and numerical simulations. Simulation results are shown to agree with measured waveforms. It is shown that carrier removal in the no-current regime of ZCS turn-off can be utilized to reduce the turn-off power loss of IGBTs in ZCS applications.

I INTRODUCTION

Maximum drive speed that can be effectively employed in traditional hard-switching environment is limited by factors like packaging, EMI noise, diode reverse recovery, etc. The use of circuit topologies exploiting soft switching [1] promises more effective utilization of semiconductor devices so that performance is limited by the semiconductor device rather than undesirable parasitics. A major hurdle in the widespread utilization of soft-switching inverter technology is the lack of optimized semiconductor devices for Zero Voltage Switching or Zero Current Switching. Commercially available IGBTs are designed for hard-switching applications. Efforts are now being made to better understand the physics of device operation under soft-switching circuit conditions so that further device optimization may be implemented. Switching dynamics of IGBTs in ZVS conditions was recently reported in literature, with the aid of numerical simulations [2]. This paper presents a study on the performance of IGBT under Zero Current Switching.

II DEVICE STRUCTURE AND TEST CIRCUIT

Fig. 1 shows the cross-section of the IGBT being used in the study. It is a punch-through device with a rating of 1200 V, 100 A. Doping density and device dimensions were extracted from the breakdown voltage of the device at room temperature. Lifetime and area were obtained from the forward I-V characteristics at room temperature. Static characteristics were then studied using an advanced two-dimensional (2-D) device simulation framework PISCES2B [3]. Fig. 2 shows the simulated and measured I-V characteristics of the IGBT at room temperature revealing close agreement between the two.

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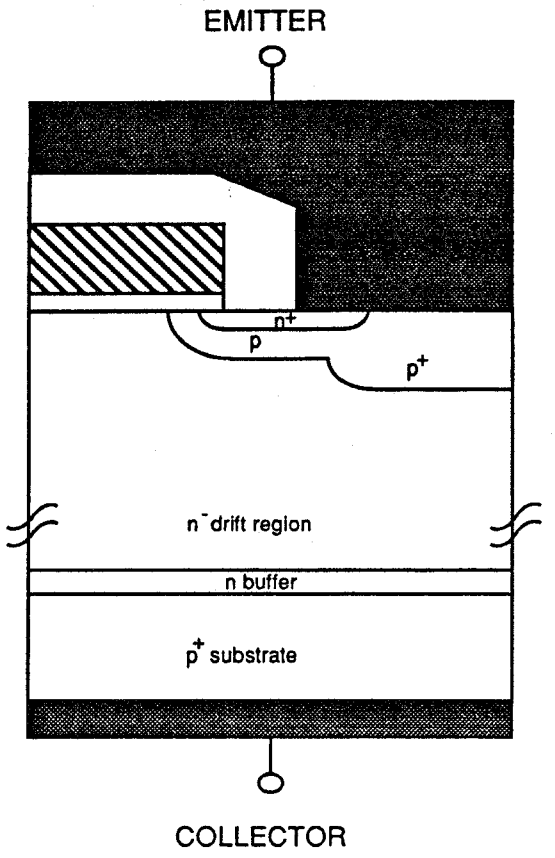


Fig. 1 Cross-section of punch-through IGBT

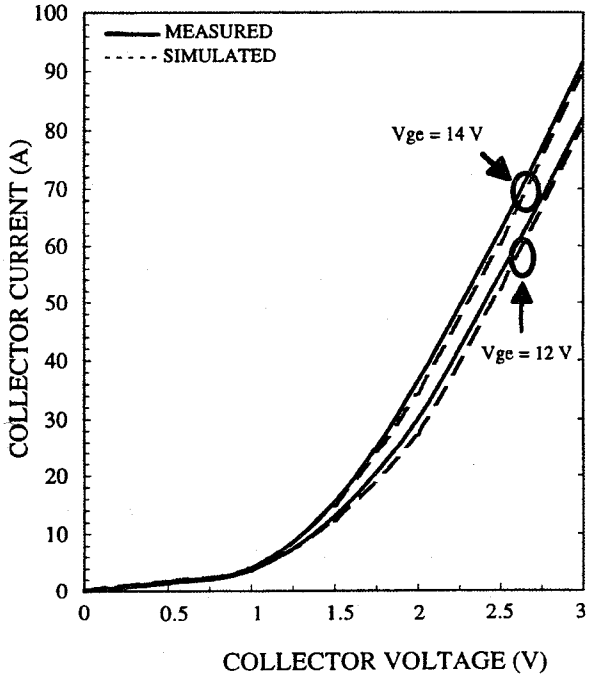


Fig. 2 Forward I-V characteristics of IGBT

The circuit, along with the gating pulses, used to study the Zero Current Switching performance of IGBT is shown in Fig. 3. The switch S and the device under test (DUT) are turned on simultaneously. The inductor L then starts charging through the device. When a desired current level is reached, the switch S is turned off. Device current abruptly falls to zero, and the inductor current now flows through the anti-parallel diode. The device can be turned-off at any time after this stage for Zero Current Switching. After the gate voltage for the DUT is removed, the switch S is turned on to complete the loop again. However, since the device has been turned off, the inductor forces current to flow through the snubber capacitor C_{snub} across the

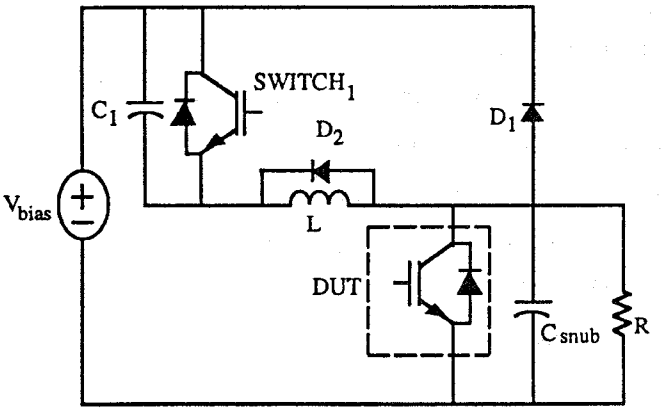


Fig. 3 (a) Circuit used to study ZCS Performance of IGBT

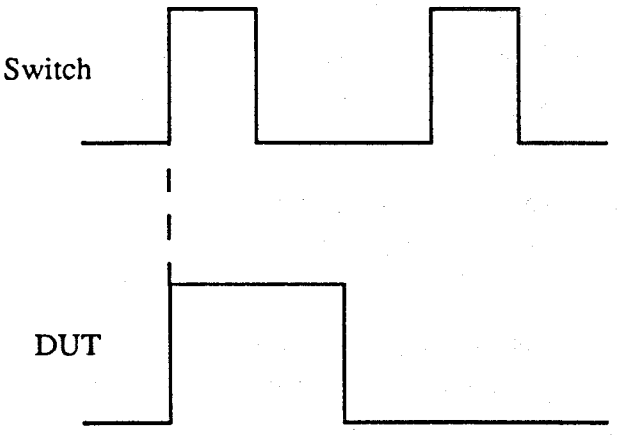
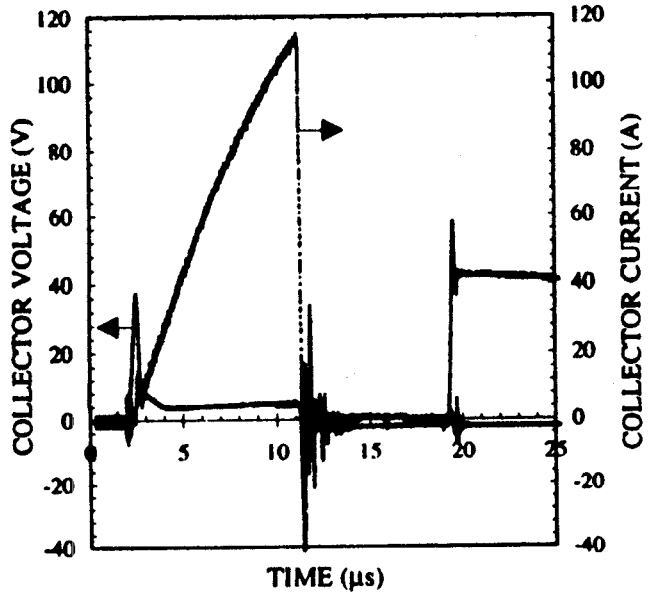


Fig. 3(b) Switching sequence for ZCS testing

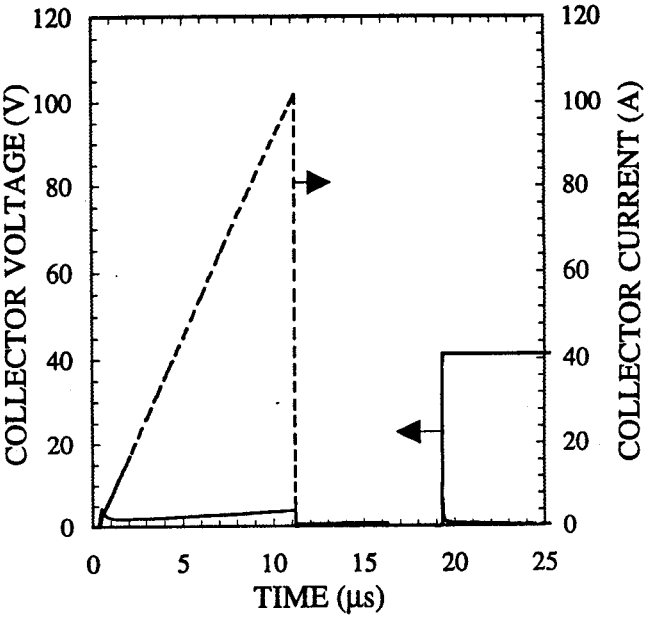
device. This inductor causes the capacitor voltage, and hence device voltage to rise linearly. Removal of charges from the drift region results in a turn-off current bump.

III RESULTS AND DISCUSSION

Typical measured and simulated ZCS switching characteristics of the IGBT are plotted in Fig. 4. A close match between the two can easily be discerned. Measured characteristics show significant ringing every time some switching is done indicating the presence of parasitics. Parasitics have not been accounted for in this study. The first gating pulse is applied simultaneously to both the switch S and the DUT. Initially the device bulk is neutral, and the device displays a turn-on voltage overshoot as the drift region enters high-level injection regime. Beyond this, the device conducts in dynamic voltage saturation [2]. Opening the switch S removes the current path through the device. Excess charges get trapped within the device and in the absence of external current, start decaying through carrier recombination. The second pulse on switch S is used to sweep out the charges in the drift region and to reset the circuit. The simulation does not include circuit parasitics and hence does not model the ringing observed in measurement.



(a)



(b)

Fig. 4(a) Measured and (b) Simulated ZCS performance of IGBT

In order to understand turn-off dynamics, device cross-section was saved at various instants during the switching, as marked as *a*, *b*, *c*, and *d* in Fig. 4(b). Instant *a* is the time instant just before switch S is opened. This is the time of maximum charge in the device. Instant *b* is the point after DUT is turned off, but before switch S is closed again. Instant *c* corresponds to the time when the device voltage reaches bus voltage. Instant *d* represents a time instant during the current tail when mnost of the charge has decayed. Decay of carriers from instant *a* to instant *d* can be seen

in Fig. 5. It is clear that there is a significant reduction in the trapped charge density from instant *a* to instant *b*. Also, there is charge re-distribution in the drift region so that the carrier profile is almost uniform. The device voltage rises rapidly between time instants *b* and *c*. This voltage is supported by the reverse biased p-base n-drift region junction. The resultant electric field sweeps out the excess charge in the drift region. Once bus voltage is reached, carriers decay in a recombination dominated phase, displaying a characteristic turn-off current tail. The device thus shows a turn-off current bump.

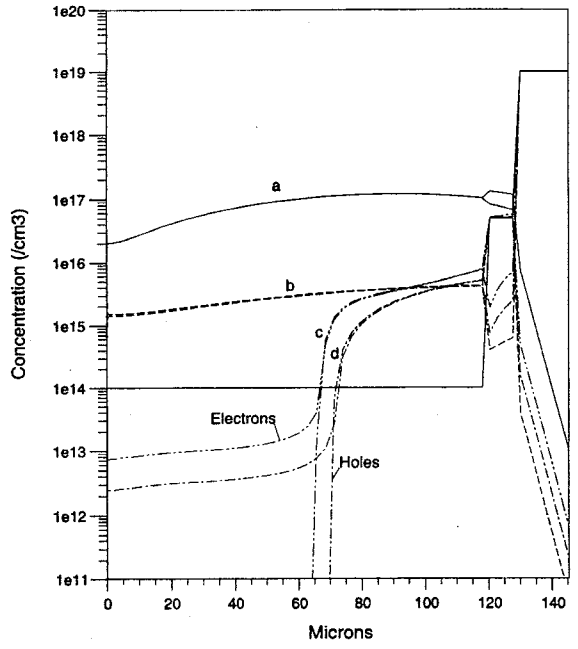


Fig. 5 Carrier concentration at various stages during ZCS turn-off

Fig. 6 shows the electron current flow vectors in the no-current regime. There is significant electron flux under the MOS gate. Further, this current flow is opposite in direction to the current direction in on-state. Also intriguing is the fact that even though electron current flows through the channel, net external current is zero.

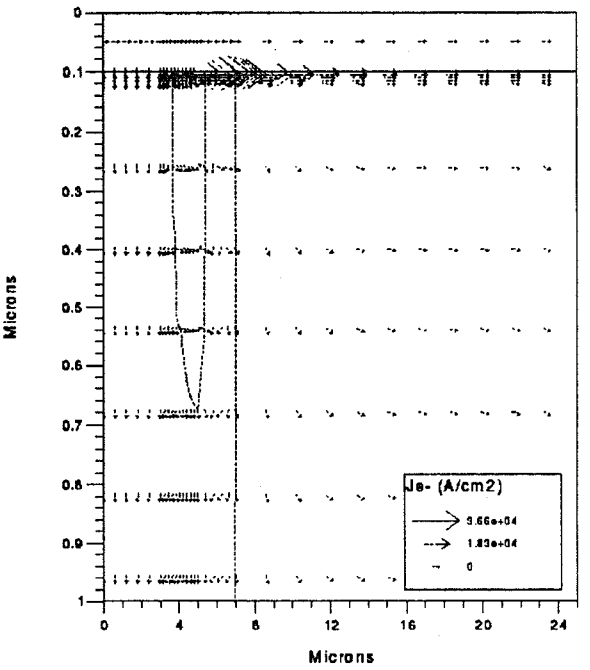


Fig. 6 Electron current vectors during no-current phase of ZCS turn-off of IGBT

In order to resolve this issue, the emitter contact was split into two contacts, one for the p^+ contact region for the base (*emitter1*) and one for the n^+ emitter region (*emitter2*). Emitter1 and emitter2 are shorted externally. The current through the collector, emitter1 and emitter2 are plotted in Fig. 7. In on-state, emitter1 conducts hole current, while emitter2 conducts electron current. As collector current ramps up, electron and hole current also increase, governed by the common emitter current gain of the vertical *pnp* transistor. When the switch S is turned off, collector current abruptly falls to zero. Due to presence of gate voltage, an inversion layer is still maintained under the gate. Excess electrons in this region are flushed out through the channel. This electron flow is due to drift-diffusion of the excess carrier in the drift region. This tends to make the carrier distribution in the drift region flatter. Simultaneously, carriers are also decaying due to recombination. This

explains the evolution of the profile *b* from profile *a* in Fig. 5. Since there can be no external current, this electron current is compensated by an equal hole

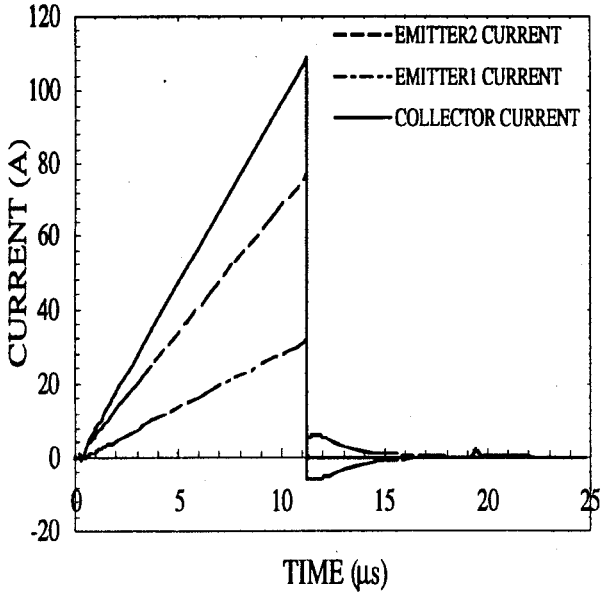


Fig. 7 Current Contributions during ZCS of IGBT

current from the p-base. Thus, both electrons and holes are swept out at the same electrode. However, once the gate voltage is removed from DUT, electron current is cut-off, which causes hole current to fall simultaneously. Remaining charges then decay by recombination. Clearly, longer is the gate voltage applied, more are the carriers swept out, and hence smaller is the turn-off bump.

IV CONCLUSION

In conclusion, Zero Current Switching performance of IGBTs has been studied using extensive measurements and numerical simulations. Significant charge removal takes place by internal carrier recombination during the phase of no current through the device. Carrier sweep-out through the channel in the no-current phase of ZCS switching can be utilised efficiently to reduce the turn-off current bump and switching time. This leads to significantly improved tail-current characteristics, and hence turn-off power loss.

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